DMA controller: (8237)

Direct Memory Access is fastest among all the modes of data transfer. Without any interferences transfers data directly to / from memory. It supports 4 DMA channels i.e., 4 peripheral devices

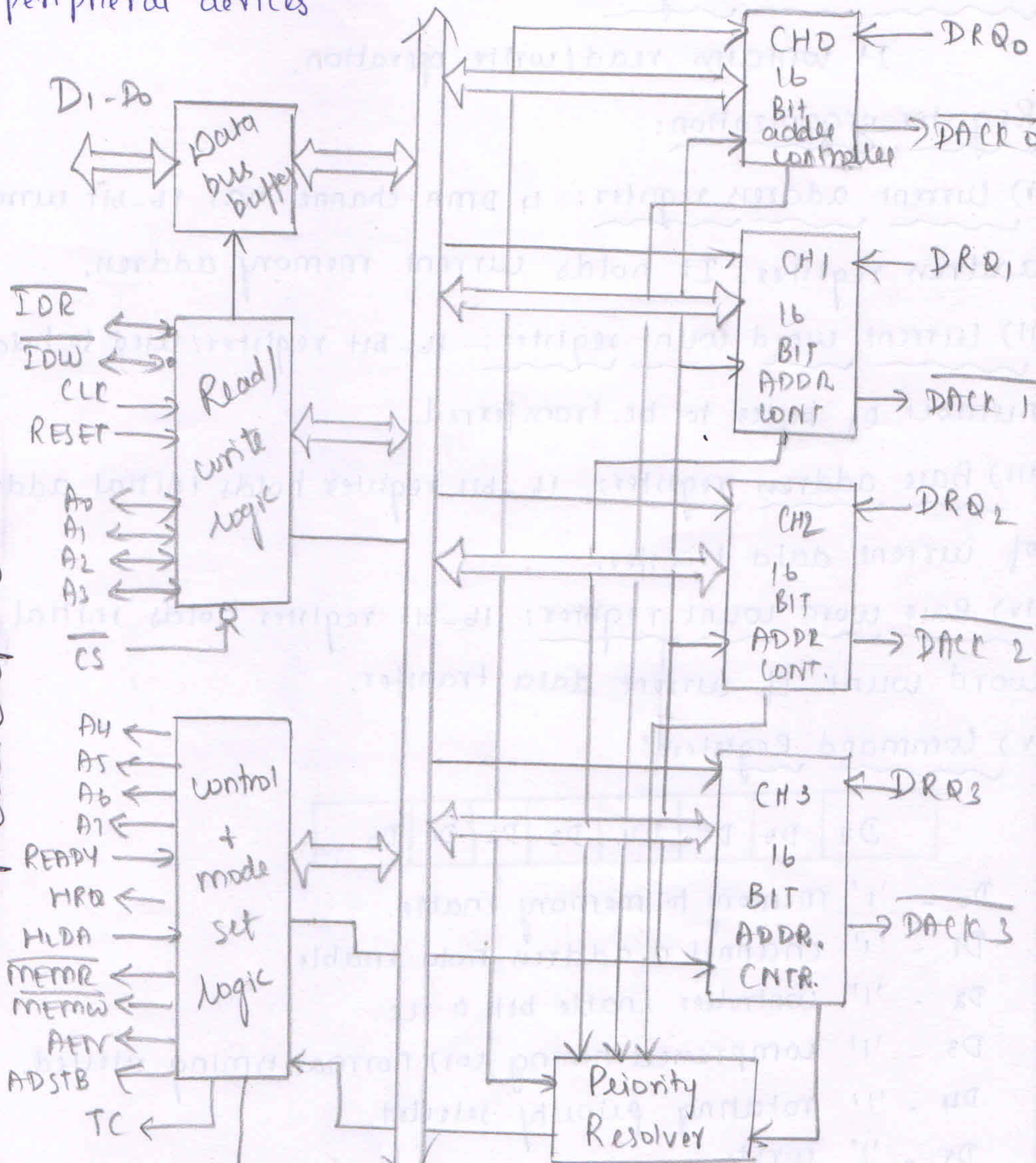


Fig: Block diagram of 8237

Data bus buffer:

8-bit bidirectional buffer. Slave mode, it transfers data between up and internal data bus. Master mode, the output A_8-A_{15} bits of memory address on data lines.

Read/write control logic:

It contains read/write operation.

Register organization:

i) Current address register: 4 DMA channel has 16-bit current address register. It holds current memory address.

ii) Current word count register: 16-bit register used to hold number of bytes to be transferred.

iii) Base address register: 16-bit register holds initial address of current data transfer.

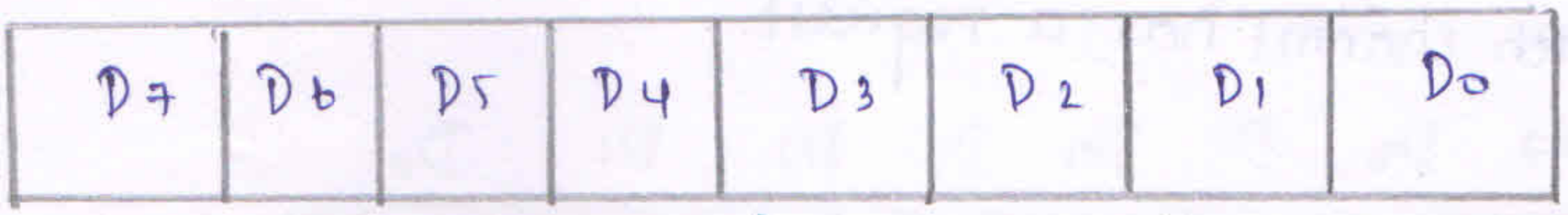
iv) Base word count register: 16-bit register holds initial word count of current data tranifer.

v) Command Register:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

D_0 - '1' memory to memory enable.
D_1 - '1' channel 0 address hold enable.
D_2 - '1' controller enable bit is set.
D_3 - '1' compressed timing (or) normal timing selected.
D_4 - '1' rotating priority selected.
D_5 - '1' write

vi) Mode set register:



Single mode:

Only one byte is transferred per request.

Burst mode:

The operation of up temporarily suspended. DMA controller sends HOLD signal to up. up suspended its operation & send HLDA. The DMA controller takes control of buses, transfer data b/w I/O devices & m/y in visible mode.

Block mode:

Block of data transferred until TC (Timing control) reached 0.

Demand mode:

This is similar to block mode.

Cascade mode:

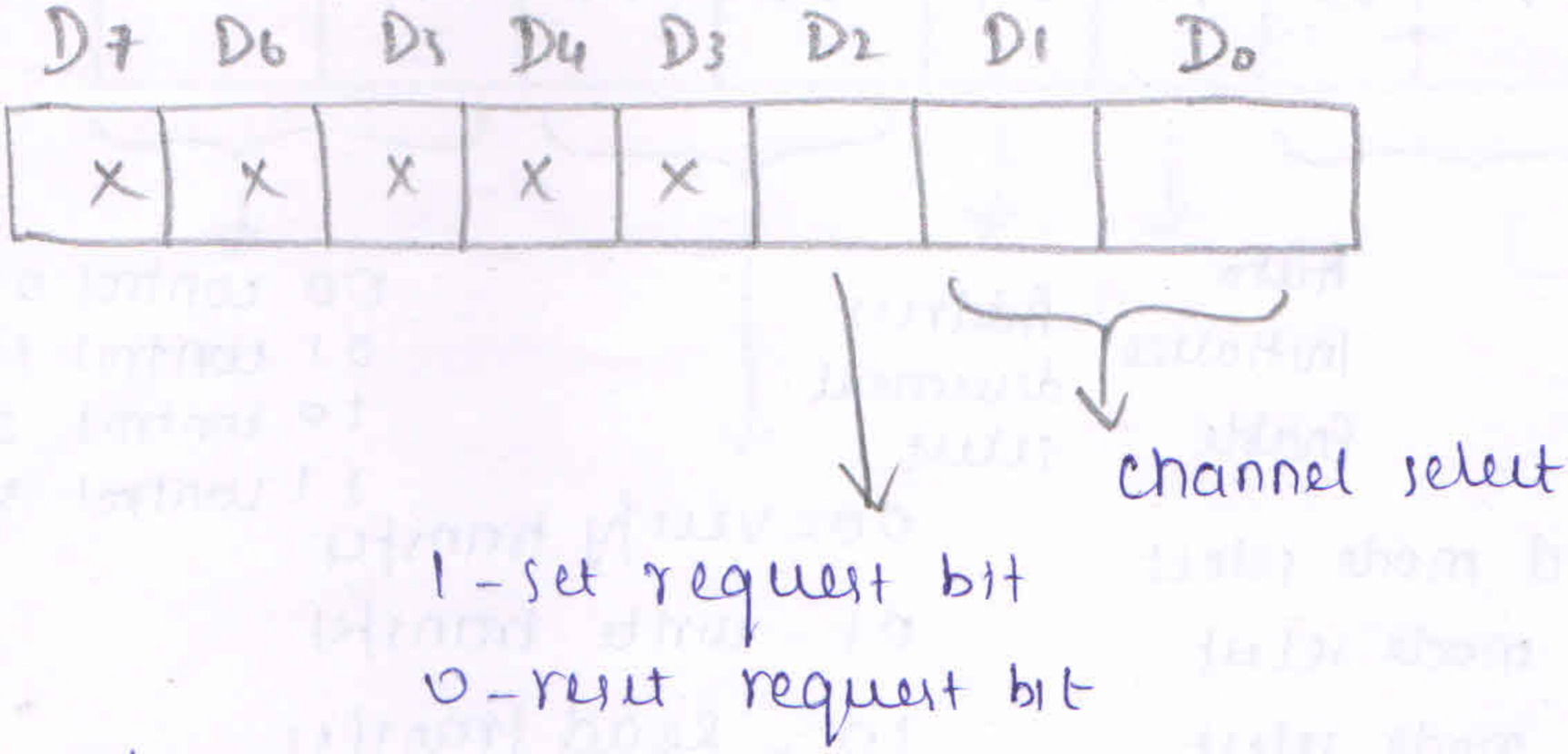
More than one 8237 connected together to provide 4 DMA channels.

Memory to memory transfer mode:

Temporary register used

vii) Request Register:

Each channel has a request.



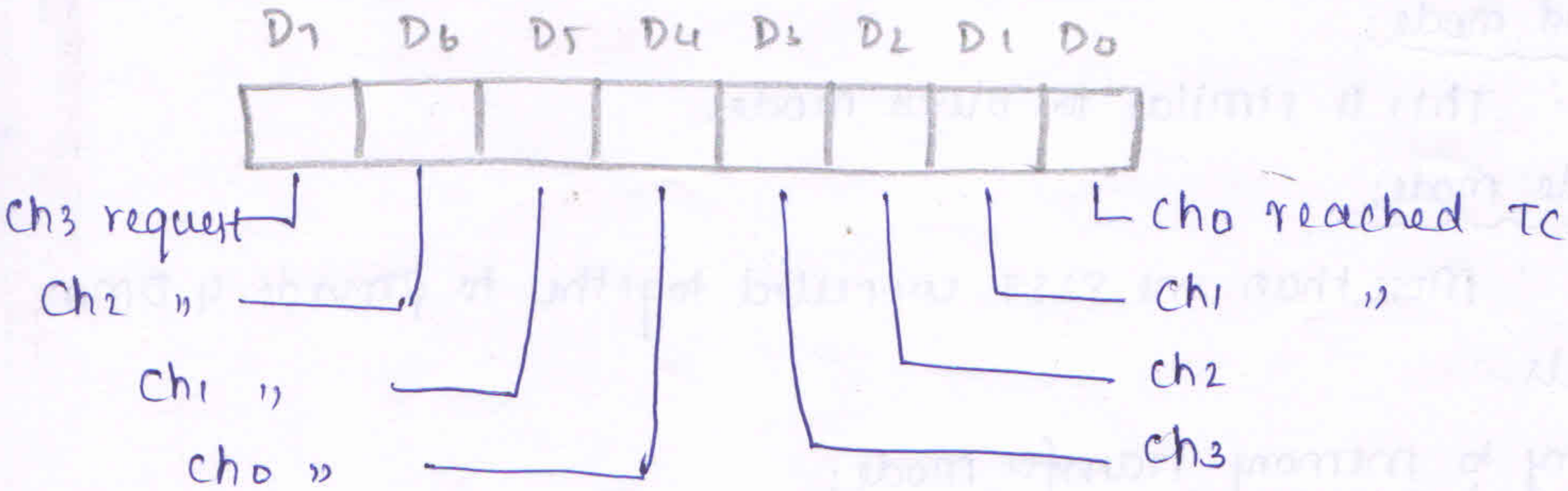
0 - reset request bit

D3 - D7 don't care.

D1	D0	
0	0	channel 0 has requested register
0	1	channel 1 "
1	0	channel 2 "
1	1	channel 3 "

viii) Mask Register:

ix) Status Register:

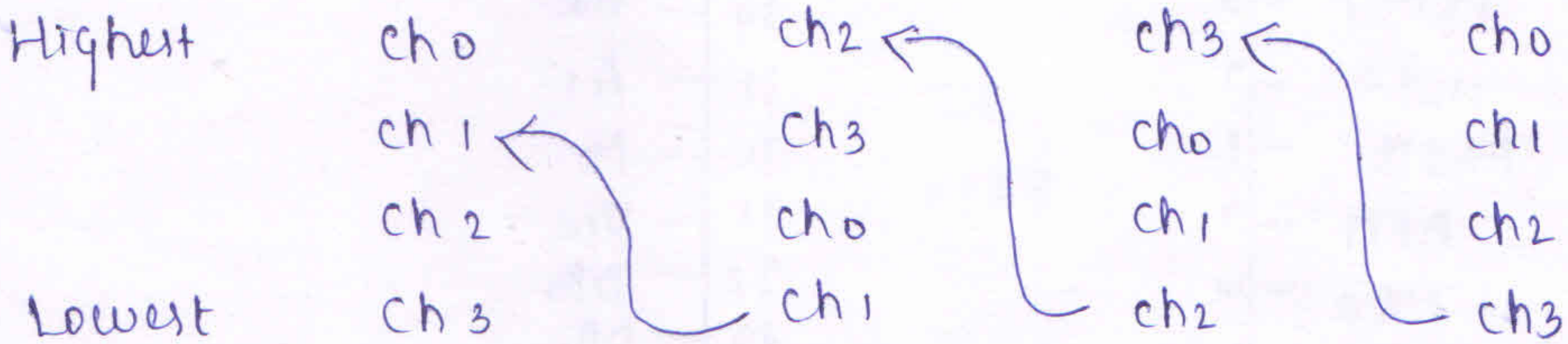


Priorities of DMA request: It has 2 priority schemes.

1) Fixed priority 2) Rotating priority.

In fixed priority, each device connected to channel is fixed. DREQ has lowest priority followed by $DREQ_2$ & $DREQ_1$ with next higher priorities while $DREQ_0$ has highes priority.

In rotating priority, channels are not fixed.



DMA transfer & operations:

1) DMA verification
2) Write operation
3) Read operation

a) A single byte transfer using 8237 requested by I/O device using DRQ inputs.

b) HLDA signal received by DMA controller that indicates available for data transfer.

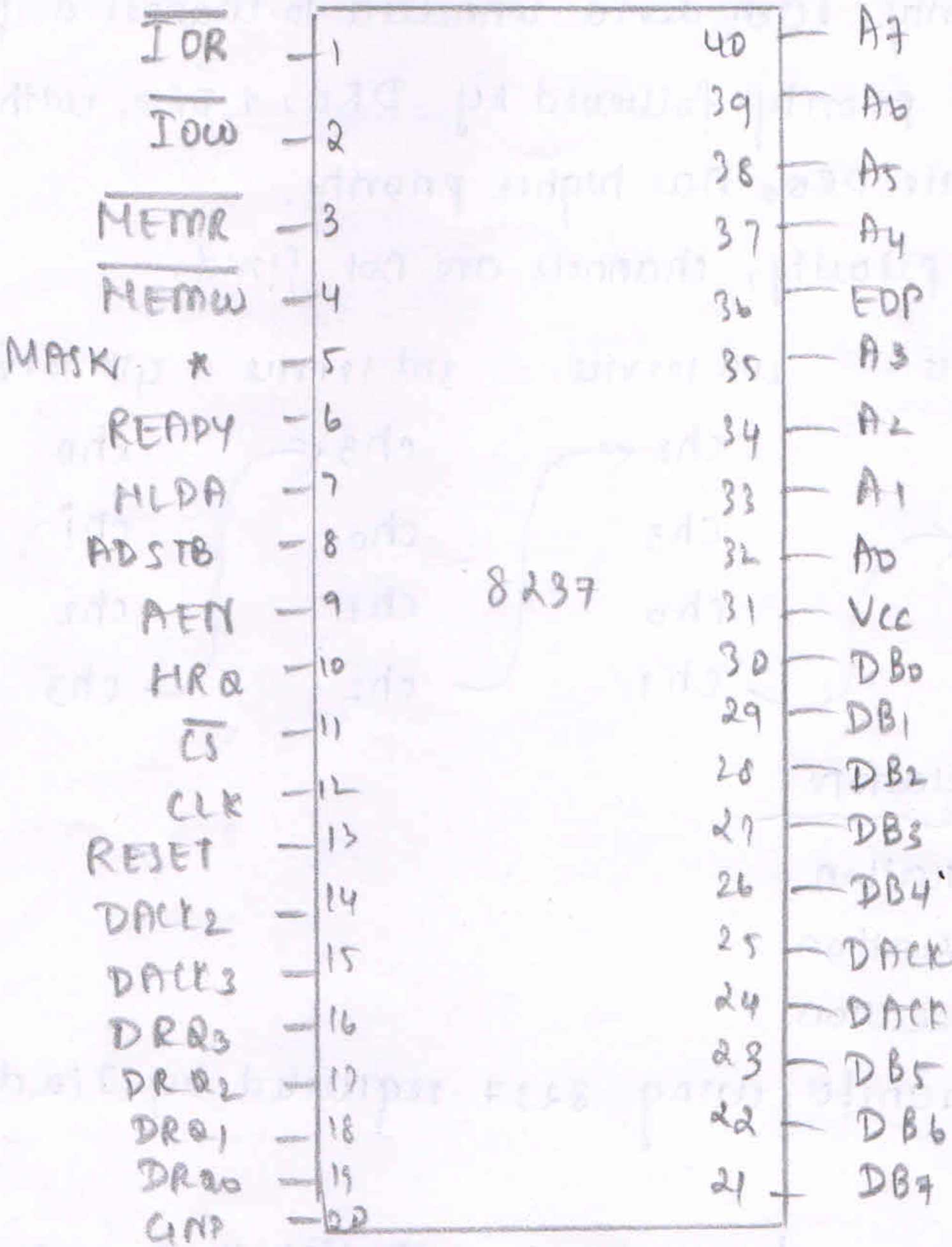
c) DACK line of the channel is pulled down.

d) DMA controller generates read & write commands

e) If more than one channel request service simultaneously transfer will occur as burst transfer.

f) The burst transfer may interrupted by external device. by pulling down HLDA line.

Fig: Pin diagram of 8237



HRQ - Hold request

CS - chip select

MEMR - Memory Read output

MEMW - Memory write output

TC - Terminal count

ADSTB - Address Strobe

AEN - Address Enable

EOP - End of operation.