# Introduction to advanced processor;

The advanced intel microprocessor are below.

i) 80186 ii) 80286 iii) 80386 iv) 80486 v) Pentium 4 + core 2.

## 80186:

80186 = 8086 + additional chips

Features:
* Memory size is 1MB.
* Local bus controller
* 2 independent high-speed DMA channels
* 3 timer + clock generator.
* programmable interrupt controller.

## 80286:

Features:
* 16 bit register + data bus, 24 bit address.
* Memory size is 16MB.
* Memory management
* Task management.
* Built in mly protection
* Protection management
* Operates in real & protected mode.

Pipelining processor Architecture includes;

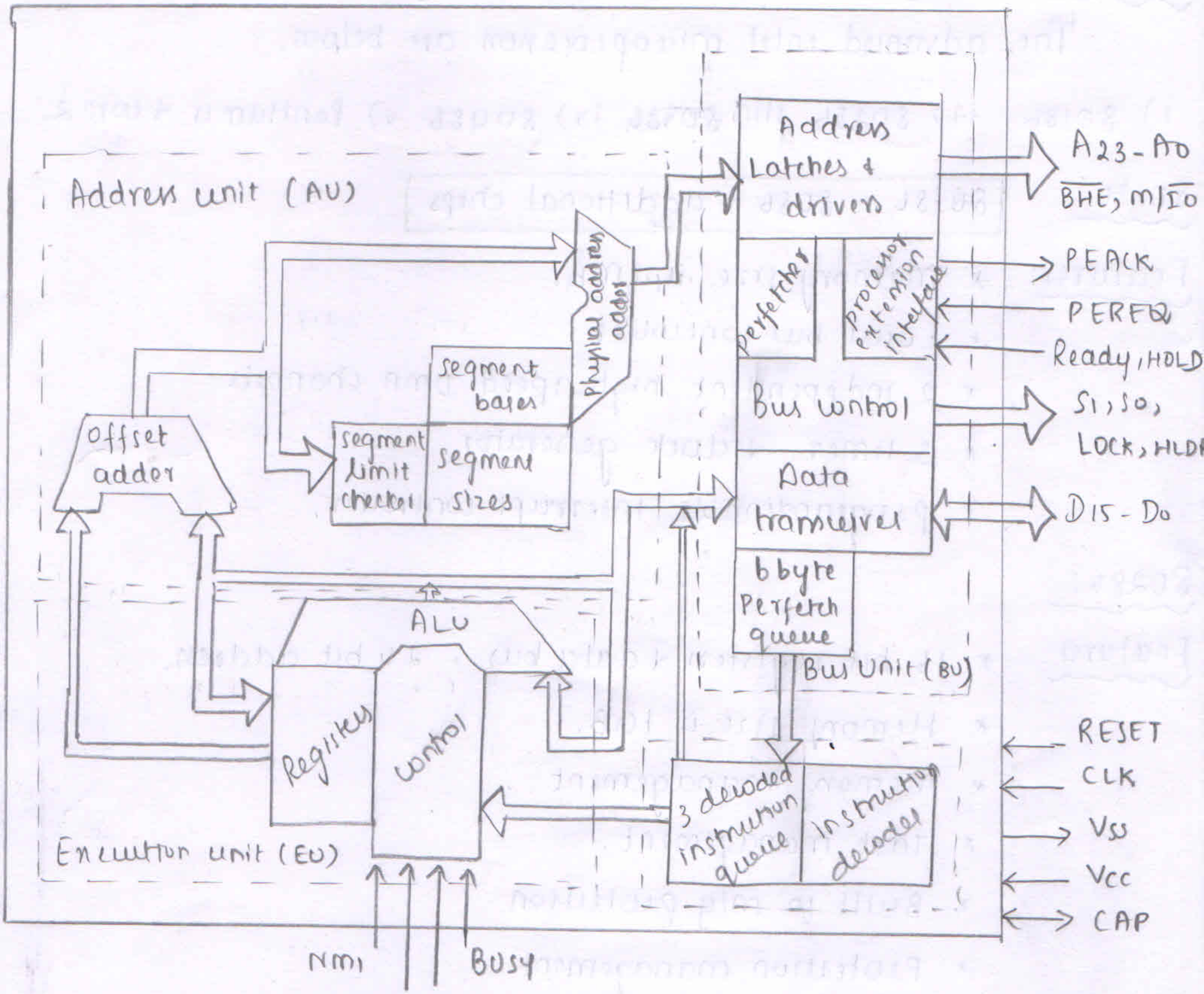
Fetching, Decoding + execution.

BU – Bus unit

AU – Address unit

EU – Execution unit

Fig : Intel architecture of 80286




80386 :

Features: * 32 bit registers, address + data bus

* Improved protected mode.

* Virtual - 86 mode.

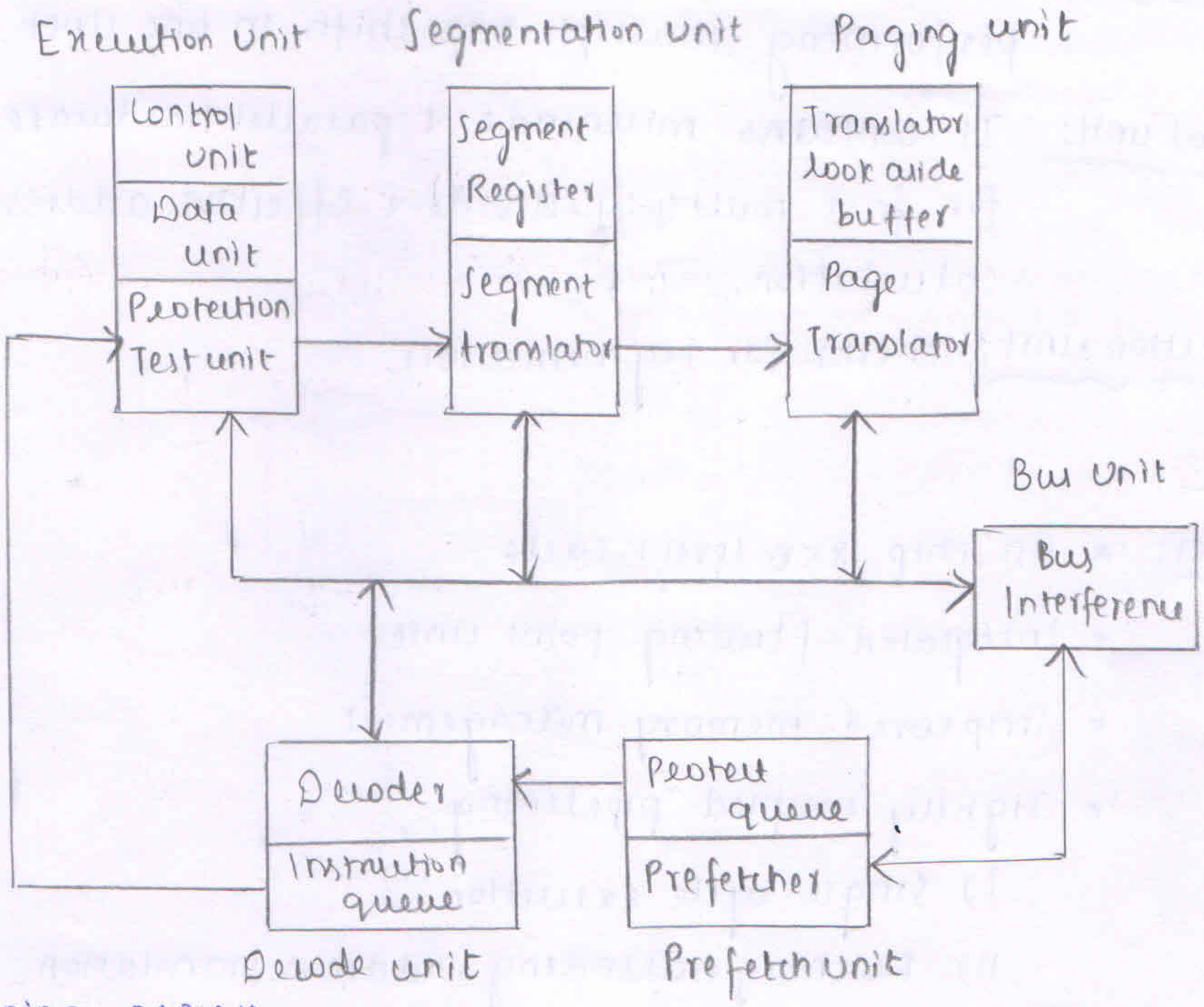
Architecture includes 3 units.

1) BIU - Bus Interface Unit

2) MMU - Memory Management Unit

3) CPU - Central Processing unit

## Fig: Internal Architecture of 80386




**Pipelining process:**

Fetching, decoding + execution.

1) **Prefetch unit:** * program look ahead function
   * 16 byte code queue.

2) **Decode unit:** * Take from prefetch queue.
   * Translate instructions
   * Store in instruction queue.

3) **Segmentation:** * Translate logical address into linear address at request of EU.

4) **Paging unit:** * The linear address sent to paging unit.

It contains

Data unit: It contains ALU, 8 GPRs, 64 bit shifter for performing multiple bits shifts in one clock.

control unit: It contains microcode + parallel hardware for fast multiply, divide + effective address calculation.

Protection unit: checks for segmentation.

80486:

Features: * On-chip 8KB level 1 cache
* Integrated floating point unit.
* Improved memory management.
* Tightly coupled pipelining.
  i) Single cycle execution
  ii) Fetching, decoding, address translation.

Pipeline process:

Code prefetch unit: * 16 byte code queue

Decode unit: * Takes from prefetch queue
* Translate instruction into microcode.

Segmentation unit: * Translate logical address into linear.
* checks for bus cycle segmentation.

Paging unit: * Translate linear address to physical address.

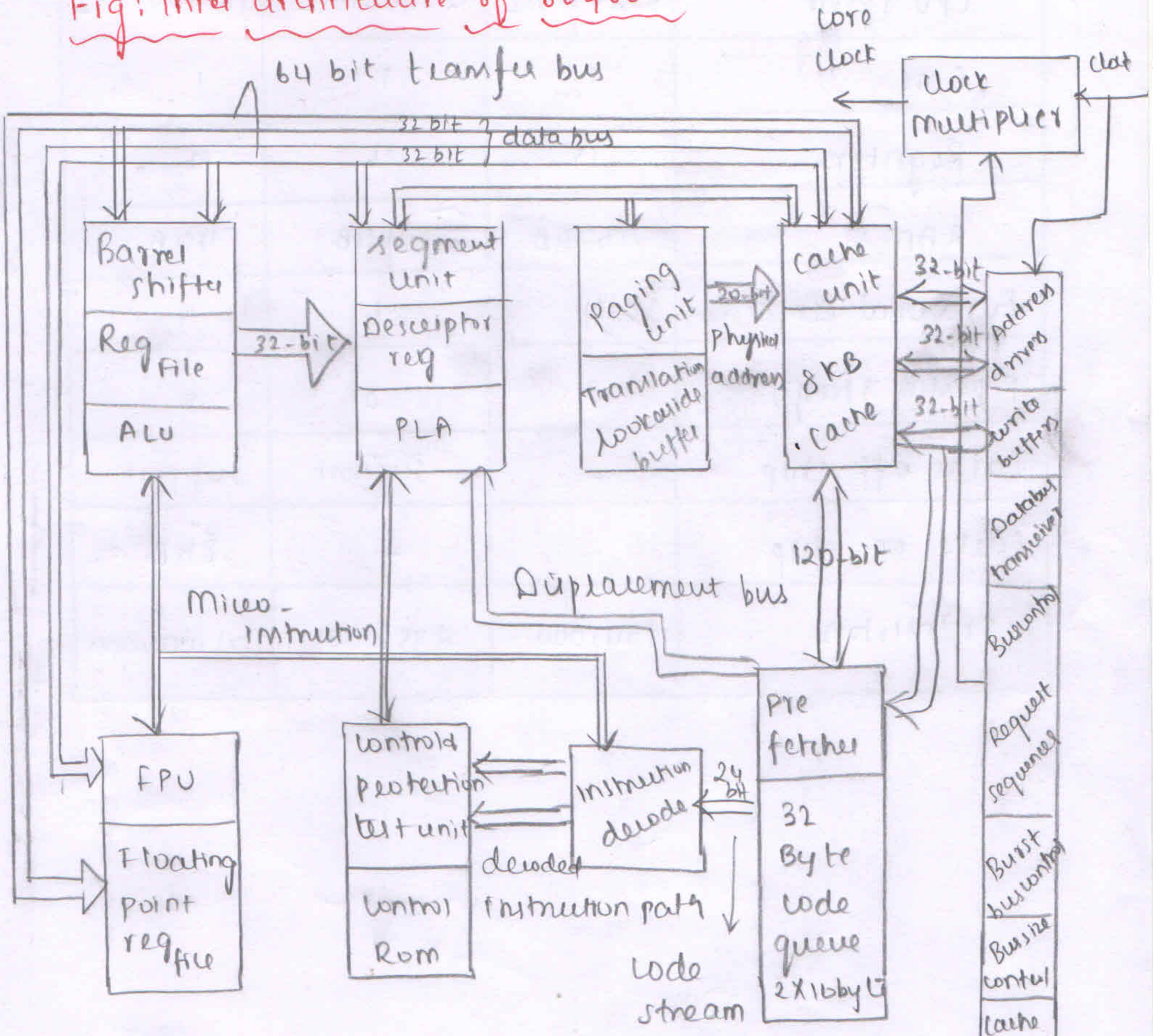
Cache unit: * closely coupled.

control unit: * controls IU, FPU, SU

Integer (or) datapath unit: * Identify where data is present.
* perform arithmetic & logical operations

Floating point unit: * Includes floating point registers, an adder, multiplier & shifter.

Fig: Intel architecture of 80486



Tab: Comparison among Intel advanced processor

| | 80286 | 80386 | 80486 |
|---|---|---|---|
| Date (or) Year | 1982 | 1985 | 1989 |
| CPU speed | 6-25 MHz | 12-40 MHz | 16-100 MHz |
| Core | 1 | 1 | 1 |
| Registers | 15 | 16 | 16 |
| RAM | 16 MB | 4 GB | 4 GB |
| Functional units | 4 | 6 | 9 |
| pipeline stages | 3 | 3 | 5 |
| Cache off chip | - | support | support |
| Cache on chip | - | - | 8 KB |
| Transistors | 134,000 | 275,000 | >1,000,000 |